Application Note 504
Design Considerations for Dallas Real-Time Clocks

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OVERVIEW

A real-time clock (RTC) allows a system to synchronize or time-stamp events to a time reference that can be easily understood by the user. Because RTCs are used in an increasing number of applications, designers should familiarize themselves with these RTCs to avoid design problems.

Selecting an Interface

RTCs are available in a wide range of bus interfaces. Serial interfaces include 2-wire, 3-wire, and Serial Peripheral Interface (SPI). Parallel interfaces include mux-bus (multiplexed data and address bus) and designs with separate address and bytewide data inputs. The choice of interface is often determined by the type of processor being used. Many processors include 2-wire or SPI interfaces. Others, such as 8051 processors and their derivatives support multiplexed address and data buses. Timekeeping NV RAMs use the same control signals as SRAMs, which many processors provide an easy interface to, and include battery-backed RAM in various densities. Finally, phantom clocks "hide" behind battery-backed RAM and use a 64-bit software protocol to gain access to the clock.

Battery Back-Up Function

In some applications, such as VCRs, the time and date information will be lost if power is removed. Many new applications require that the time and date remain valid even if the main power supply is removed. To keep the clock oscillator running, a primary or secondary battery or large capacitor may be used. In this case, the RTC must be able to switch between the two power supplies.

If a primary battery, such as a lithium coin cell, is used for back-up, the RTC should be designed to draw as little power as possible when running from the battery. The switching circuitry, normally powered from the main supply pin, will switch to the battery and put the RTC into a low power mode. Communications between the microprocessor and the RTC are usually locked out (often called write protect) to keep the battery current at a minimum and to prevent data corruption.

Many clocks include an oscillator control bit, usually called the clock halt (CH) or enable oscillator (/EOSC) bit. This bit is usually located in bit 7 of the seconds register, or in a control register. In almost all clocks with this bit, the preferred state upon initial battery attach is for the oscillator to be off. This allows the system designer to set up a manufacturing flow such that, after assembly and test, the Vbat supply, normally a lithium battery, is installed. The oscillator will be in the off state, conserving the battery until the system is powered up. At that point, the firmware/software should start the oscillator and prompt the operator for the time and date.

Most Dallas products that include a battery input pin include on-chip reverse charging protection circuitry. Regulatory agency data and Conditions of Acceptability information can be found at www.maxim-ic.com/TechSupport/QA/ntrl.htm.

Lithium batteries are normally rated to operate from -40ºC to +85ºC. The battery should never be exposed to temperatures above +85ºC. Packages that include the battery and have exposed battery pins, such as the SmartSockets, should never be water washed. Water washing will short the battery terminals, therefore draining the batteries.

CLOCK MODULES, FRESHNESS SEAL AND SHELF LIFE

The majority of the current consumed by a clock while in battery-backed mode is from the oscillator. All clock modules with embedded crystals and batteries are shipped from the factory with the oscillator disabled. The battery current while the oscillator is disabled is less than the self-discharge of the battery, or about 0.5% per year at room temperature.

Some timekeeping NV RAM modules use a clock-controller IC and a SRAM. The oscillator is disabled and the SRAM is electrically disconnected from the battery when shipped from the factory. The battery will be connected to the SRAM after Vcc is removed for the first time. This function is often called "freshness seal," and is used to conserve the battery until the module is first used. Other timekeeping NV RAM modules are monolithic (controller and SRAM in one IC) and require no freshness seal.

Module Packages

Timekeeping NV RAMs, mux-bus clocks, and some watchdog and phantom clocks are available in module and/or PowerCap® packages. Modules include an embedded 32,768 Hz crystal and a lithium battery, making PCB design easier. However, crystals and batteries cannot tolerate the temperatures encountered during the reflow process. Modules may be attached manually or inserted in a socket after reflow. Modules may also be attached to the PCB using wavesolder, as long as the lithium battery is not exposed to temperatures above +85ºC.

PowerCap products use a two-piece construction to provide a device that can be surface-mounted using the reflow process. The module base, containing the RAM and clock, is mounted to the board using standard reflow techniques. The PowerCap top, containing the heat sensitive battery and crystal, is snapped onto the base after soldering.

Clock Format

There are three major data formats used in RTCs: binary-coded decimal (BCD), binary with separate registers for the month, date, year, etc., and unformatted binary counters.

The BCD format is the most common. One reason for its popularity is that the time and date can be easily displayed in a human-readable format with no "conversion." Each 8-bit register represents two digits (one nibble per digit). Each 4-bit nibble can hold the binary representation of the digits 0 thru 9. An example of the register map for a typical BCD format clock is shown in Figure 1.

Since some of bits are not needed for a particular time or date field, those bits can be used for special functions, general-purpose read/write bits, or can be hardwired to read back as always one or zero, depending upon the design. In Figure 1, bit 7 of the seconds register is used for the clock halt (CH) bit.

The second format is the binary format, with separate registers like the BCD format. The binary format is normally a programmable option on some clocks with the BCD format

The third format uses a single multibyte register representing the time in seconds in an unformatted binary value from some reference point.

PowerCap is a registered trademark of Dallas Semiconductor.

Figure 1. **TYPICAL TIME AND DATE REGISTER MAP**

Address	Function	Data Range	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
00H	Seconds	00-59	CH	10 Seconds			Seconds			
01H	Minutes	00-59	X	10 Minutes			Minutes			
02H	Hours	00-23	X				Hours			
03H	Day	1-7	X	X	X	X	X	Day		
04H	Date	01-28/29/30/31	X	X	10 Date		Date			
05H	Month	01-12	X	X	X	10 Month	Month			
06H	Year	00-99	10 Year				Year			
07H	Control	varies								

The time and date registers are updated once per second. The roll-over value for the date will vary depending upon the month and for February, by year. The day register, except for mux-bus clocks, is not tied to any other register. The day register will increment at midnight, and will roll over from 7 to 1. The programmer can select any particular day as “1,” as long as the assignment is consistent throughout the program. On mux-bus clocks, Sunday must be “1” because the day register is used for the daylight savings test. The test for daylight savings is done at midnight on the preceding midnight roll-over, which must be accounted for when testing the daylight savings function.

When changing from 12-hour mode to 24-hour mode, or from BCD to binary or binary to BCD, the time, date, and alarm registers must be re-initialized.

Unformatted binary counter clocks have a single register, typically 32-bit, that is incremented once per second. Normally, a value of 00h in the register is considered to be some default time and date, e.g., the “zero epoch” value of 00:00:00 January 1, 1970 GMT. The binary value in the register then represents the elapsed time from that point. Software routines must be used to convert the 32-bit value to a readable time and date, and to convert user entries to a binary value.

Y2K Compliance

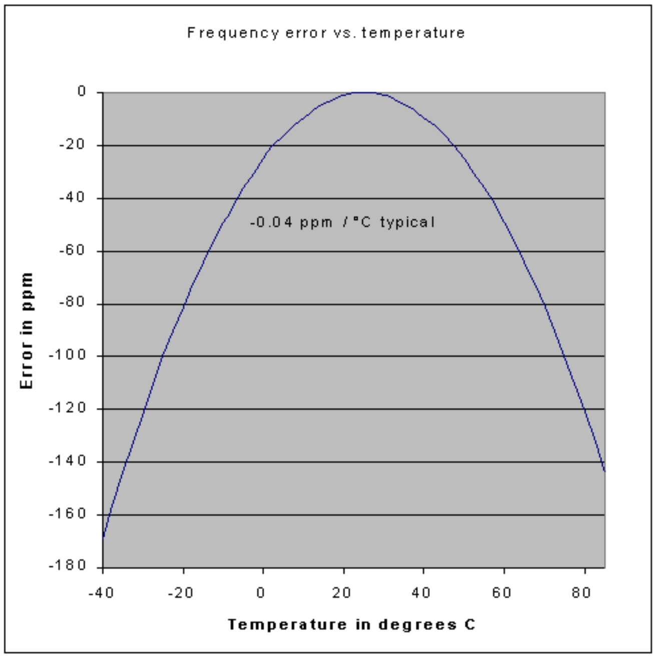
Dallas Semiconductor RTCs are either Y2K compliant, Y2K compatible, or do not contain date-sensitive logic. A Y2K-compliant clock has logic that includes century information (either century digits or a century bit) and correctly calculates the leap year through 2099. Y2K-compatible clocks correctly calculate the leap year through 2099, but requires the system software to track the century. Binary seconds clocks do not have date sensitive logic; the software must calculate the correct date, including leap year corrections.

Crystals and Accuracy

The crystal oscillator is one of the most accurate circuits available for providing a fixed frequency. A 32,768Hz crystal is used for most RTCs. By dividing down the output of the oscillator, a 1Hz reference can be used to update the time and date. The accuracy of the RTC is dependent mainly upon the accuracy of the crystal. Tuning fork crystals have a parabolic frequency response across temperature (Figure 2). An error of 23ppm is about 1 minute per month.

Crystals are tuned to oscillate at the correct frequency under a particular capacitive load. Using a crystal tuned for a 12.5pF load on an RTC designed to present a 6pF load to the crystal will result in the clock running too fast.

Figure 2. **CRYSTAL ACCURACY VS. TEMPERATURE**



Crystal Connections

All Dallas RTCs have internal bias networks. The crystal should be connected directly to the X1 and X2 pins, with no additional components (Figure 3). The crystal should be as close as possible to the X1 and X2 pins. A ground plane should be placed beneath the crystal, X1 and X2 (Figure 4). Digital signal lines should be routed away from the crystal and oscillator pins. Components that radiate significant levels of RFI should be shielded and located away from the crystal. Low-power crystal-oscillator circuits can be sensitive to nearby RFI, which can cause the clock to run fast.

Figure 3. **RTC-EQUIVALENT CIRCUIT SHOWING THE INTERNAL BIAS NETWORK**

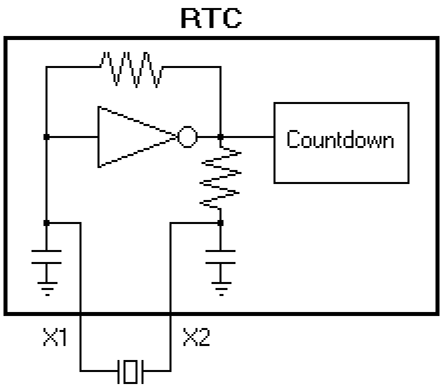
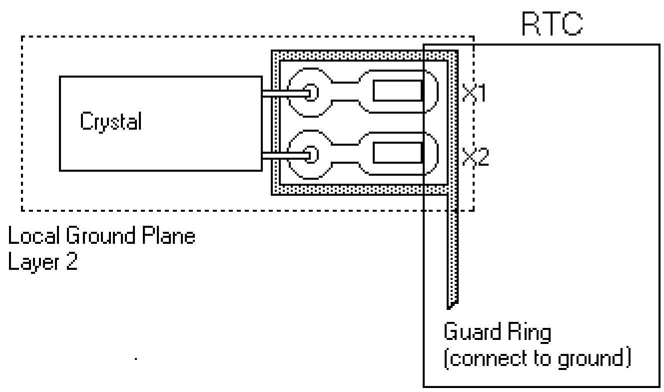


Figure 4. **RECOMMENDED LAYOUT FOR CRYSTAL**



PC boards containing tuning-fork crystals, such as those used with RTCs, should not be cleaned using ultrasonics. The crystal can be damaged by resonance vibration.

Oscillator Start-Up Time

Oscillator start-up times are highly dependent upon crystal characteristics and layout. High ESR and excessive capacitive loads are the major contributors to long start-up times. A circuit using a crystal with the recommended characteristics and following the recommended layout will usually start within one second.

Battery Connections

Most Dallas RTCs include a battery input pin. The battery is intended to keep the RTC running while the main supply is off. For most of the designs, the battery is intended to be a lithium-type coin cell.

Some RTCs use the battery voltage as a reference to determine when V_{CC} is at a valid level. When V_{CC} is below the minimum value, the part will go into write protect, locking out access to the part. While the RTC is operating from V_{CC}, the V_{BAT} input will be at a high impedance. If a battery is not connected to the V_{BAT} input, or is connected with diodes in series, the V_{BAT} input can float high, causing the RTC to go into write protect. Reverse charging protection is provided internally on most Dallas clocks, eliminating the need for external diodes. Check the following link for information about UL approval of the reverse charging protection: www.maxim-ic.com/TechSupport/QA/ntrl.htm.

Reading and Writing the Time and Date

Most Dallas clocks provide a method to ensure that the time and date registers can be accessed without the values getting corrupted due to an internal register update while the read or write is in progress.

A second set of registers (secondary buffer registers) are used on some serial clocks. When the RTC is accessed (Read), the current time and date are transferred to the secondary registers. A burst read will take the data from the secondary registers, which remain unchanged while the internal registers continue to update. The next access (when chip enable, RST, or Start occurs) will transfer the data again. A similar process happens when the registers are written, except that the data does not get transferred until the end of the access.

On timekeeping NV RAM clocks, either a TE bit or (R)ead and (W) bits are used to “freeze” the user registers.

On mux-bus clocks, several methods are available to ensure that the time and date registers do not change while being accessed. The following methods are available:

Set Bit

When the SET bit in register B is set to a one, the user copy of the double buffered time and date registers is latched. The internal registers continue to update normally.

UIP Fag

The Update In Progress (UIP) flag will pulse once per second. After the UIP bit goes high, the update transfer occurs 244µs later. If a low is read on the UIP bit, the user has at least 244µs to read the time and date and avoid errors due to an update.

UF Interrupt

If enabled, an interrupt occurs after every update cycle that indicates that over 999ms are available to read valid time and date information.

Default Register Values

Unless otherwise noted in the datasheet, the initial power up register values are undefined. That is, they should be treated the same as DRAM or SRAMs: On initial power up, the data will for practical purposes be random.

TROUBLESHOOTING NEW DESIGNS

Cannot Communicate with the RTC

When trouble-shooting a new design, there are several methods that can be used to help identify the cause of the problem. If, for instance, it appears that the part is not responding at all, it is usually worthwhile to try to determine if the part will not read, write or both. If the part has a software-enabled feature such as a square wave out, attempting to enable that feature would be a good way to determine if you can write to the part. On 2-wire parts, an oscilloscope can be used to verify if the clock is sending an acknowledge at the end of each byte. The following paragraphs describe some additional trouble-shooting hints.

Battery-backed RTCs use a comparator to switch between V_{CC} and V_{BAT}. Some RTCs use the battery voltage as the reference, while others will use a bandgap voltage reference to determine when V_{CC} is valid. Once V_{CC} drops below the comparator trip point, read and write access is not possible. Preventing access below a certain voltage helps to prevent inadvertent writes from a processor that no longer has a valid supply. Also, When V_{CC} is above the trip point, the comparator switches the internal circuits to V_{CC}, preventing battery drain. On battery voltage based referenced devices, a floating battery input, an input with a diode between the battery and V_{BAT}, or a battery with too high of a voltage can prevent communications with the RTC. Make sure that V_{BAT} is at a valid level and that there are no diodes between the battery and the battery input pin.

Serial clocks require that the “command byte” or “slave address” be written to the device correctly. An incorrect command/address often results in the device ignoring read routines. In those cases, the data I/O pin stays in a high-impedance state. On a serial bus with pull up resistors, the data read back will usually be 0xff. On 3-wire interfaces, if the I/O pin has an internal pull-down resistor, the data will often be 0. In other cases, the data read back will often be whatever value the last bit of the command byte was. Some serial clocks use a separate supply input for the outputs, to allow interfacing to processors running at a lower supply voltage. Failure to connect a valid supply to the input will keep the I/O pin from driving high. Finally, data out may be all ones or zeros if the software does not switch the microprocessor’s port pin that is connected to the clocks I/O pin from an output (while writing the command byte) to an input (for reading data from the clock.

Invalid Time and Date Values

Most time and date registers can accept any value, including invalid ones. If an invalid value is entered into a register, the value will increment until the bits used for comparison for rollover match. The value will then roll over to the minimum value. Invalid values can also be caused if the clock is in the wrong mode, i.e., binary instead of BCD, or 12 hour instead of 24.

Data Loss/Data Corruption

Data loss is usually caused by one of two things: inadvertent writes to the clock, or negative voltage “glitches” being applied to the IC. Data loss caused by negative voltage inputs to the IC can sometimes be identified because the CH or /EOSC bit (on clocks with an oscillator control bit) will be in their default “halt” state. Additionally, the data in most if not all of the registers will be corrupted. Inadvertent writes normally occur during power cycling as well, but will usually only affect one register. It usually does not affect serial clocks.

Many modern switching power supplies will, on power-up and/or power-down, create a voltage spike on V_{CC}, often going negative by five or six volts or more. This negative voltage will couple onto the internal supply of the clock via input protection diodes. If the power supply can source more current than the battery, data will be lost. In some cases, a Schottky diode can be used to clamp the negative voltage spike.

Another source of negative voltages on the clock can come from RS232 connections. If the PCB with the clock IC is powered down, and a powered PC or other instrument is connected to that board via an RS232 connection, the RS232 transceiver IC(s) may pass the negative marking voltage on to other ICs on the unpowered board.

Inadvertent writes also cause data corruption problems. The processor can write incorrect data during power-up or power-down, before write protect switches in. The interface circuitry may force the input pins into a write condition upon power-up or power-down. In the case of mux-bus clocks, the address information is latched in on the falling edge of ALE. If /WE and /CS go low before the part is in write protect, the data in the last register that was last accessed will be corrupted. V_{CC} rise and fall times should be verified that they meet the datasheet requirements.

Intermittent data problems have been caused by interrupts routines that are not handled correctly. In some cases, the time and date information is copied to RAM, and the copies are not kept in sync. Finally, In-Circuit Emulator (ICE) hardware can be configured improperly, causing erratic behavior.

Oscillator Problems

The most common reason for the clock to not increment is that the oscillator has not been enabled. Most Dallas clocks have a bit, usually located in the seconds register, that must be set before the oscillator will run.

The oscillator circuit is designed to be low power, to prolong battery life. Problems with the crystal connection can decrease the loop gain, preventing the oscillator from running. External capacitors connected to the crystal will reduce the loop gain, and increase the start up time, or prevent oscillation. Oscilloscope probes can also prevent oscillation. Crystals with an ESR above 45k? will also decrease the loop gain. Finally, some water-wash solder fluxes can appear to leave the PCB clean, while leaving enough contaminates to prevent oscillation.